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10/068,293	02/06/2002	Hee Wong	NATI15-05132	9652

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EXAMINER	
LE, DUY K	

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2685	

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/068,293	Applicant(s) WONG ET AL.	
	Examiner Duy K Le	Art Unit 2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, 7-11, 13, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0160740 A1 to Hatcher et al. in view of Ishihara (U.S. Patent Application Publication 2001/0016017 A1).

As to claim 1, Figure 2 in Hatcher shows a radio frequency (RF) down/up conversion circuit (108) comprising:

a differential radio frequency (RF) mixer (204) having a first differential input port (214, 216) capable of receiving said product signal from said multiplier and a second differential input port (206, 208) capable of receiving a first differential modulated radio frequency (RF) signal and a second differential modulated radio frequency (RF) signal, wherein said differential RF mixer generates a differential output signal (218, 220) (see page 3, col. 1, paragraph [0031], lines 1-13, and paragraph [0032], lines 1-11).

However, it does not disclose a local oscillator chopping circuit comprising: a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and a multiplier capable of

receiving said first and to second LO signals and generating a product signal of said first and second LO signals.

The Ishihara reference teaches a local oscillator chopping circuit (30) comprising: a frequency divider circuit (31) capable of receiving a first local oscillator (LO) signal (40) having a frequency of LO and generating therefrom a frequency divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal (see page 3, col. 2, paragraph [0041] and Figure 6); and a multiplier (32) capable of receiving said first and second LO signals and generating a product signal of said first and second LO signals (see page 3, col. 2, paragraphs [0042] to [0044], and Figure 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Hatcher to comprise a local oscillator chopping circuit comprising: a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and a multiplier capable of receiving said first and to second LO signals and generating a product signal of said first and second LO signals, as taught by Ishihara, in order to generate a carrier frequency which is different from the oscillation frequency and does not affect the oscillation frequency in the case of feedback of the output digital carrier signal.

As to claims 2 and 11, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 1 and 10 wherein said multiplier is an analog multiplier (see page 3, col. 2, paragraphs [0042] to [0044], and Figure 6).

As to claims 4, 13, and 20, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 1, 10, and 19 wherein said differential output signal of said differential RF mixer is a double-sideband suppressed carrier signal (Hatcher: see page 3, col. 2, lines 5-6 and paragraph [0036], and Figure 3). The mixer is a double-balanced mixer that functionally generates double-sideband suppressed carrier signal).

As to claims 7 and 16, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 1 and 10 wherein said differential RF mixer comprises a first differential pair of transistors comprising a first transistor and a second transistor, wherein a base of said first transistor is coupled to a first differential output signal received from said multiplier, and an emitter of said first transistor is coupled to an emitter of said second transistor and a to said first differential modulated radio frequency (RF) signal (Hatcher: see page 3, col. 2, lines 5-6 and paragraph [0036], and Figure 3).

As to claims 8 and 17, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 7 and 16 wherein said differential RF mixer comprises a second differential pair of transistors comprising a third transistor and a fourth transistor, wherein a base of said third transistor is coupled to a second differential output signal received from said multiplier, and an emitter of said third transistor is coupled to an emitter of said fourth transistor and to said second differential modulated radio frequency (RF) signal (Hatcher: see page 3, col. 2, lines 5-6 and paragraph [0036], and Figure 3).

As to claims 9 and 18, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 8 and 17 wherein a collector of said first transistor is coupled to a collector of said third transistor to form a first differential output signal of said

differential output signal generated by said RF mixer and wherein a collector of said second transistor is coupled to a collector of said fourth transistor to form a second differential output signal of said differential output signal generated by said RF mixer (Hatcher: see page 3, col. 2, lines 5-6 and paragraph [0036], and Figure 3).

As to claim 10, Figure 2 in Hatcher shows a radio frequency (RF) receiver (108) comprising:

a receiver front-end circuit (202) capable of receiving an incoming RF signal from an antenna and filtering and amplifying said incoming RF signal (see page 2, col. 2, paragraph [0030]); and

a radio frequency (RF) down/up conversion circuit coupled to said receiver front end circuit comprising:

a differential radio frequency (RF) mixer (204) having a first differential input port (214, 216) capable of receiving said product signal from said multiplier and a second differential input port (206, 208) capable of receiving a first differential modulated radio frequency (RF) signal and a second differential modulated radio frequency (RF) signal, wherein said differential RF mixer generates a differential output signal (218, 220) (see page 3, col. 1, paragraph [0031], lines 1-13, and paragraph [0032], lines 1-11).

However, it does not disclose a local oscillator chopping circuit comprising: a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and a multiplier capable of

receiving said first and to second LO signals and generating a product signal of said first and second LO signals.

The Ishihara reference teaches a local oscillator chopping circuit (30) comprising: a frequency divider circuit (31) capable of receiving a first local oscillator (LO) signal (40) having a frequency of LO and generating therefrom a frequency divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal (see page 3, col. 2, paragraph [0041] and Figure 6); and a multiplier (32) capable of receiving said first and second LO signals and generating a product signal of said first and second LO signals (see page 3, col. 2, paragraphs [0042] to [0044], and Figure 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the receiver of Hatcher to comprise a local oscillator chopping circuit comprising: a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and a multiplier capable of receiving said first and to second LO signals and generating a product signal of said first and second LO signals, as taught by Ishihara, in order to generate a carrier frequency which is different from the oscillation frequency and does not affect the oscillation frequency in the case of feedback of the output digital carrier signal.

As to claim 19, it is a method of claim 1, thus what is cited in claim 1 is applicable to claim 19.

3. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0160740 A1 to Hatcher et al. in view of Ishihara (U.S.

Patent Application Publication 2001/0016017 A1) and further in view of McGuffin et al. (U.S. Patent 3,922,593).

As to claims 3 and 12, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 1 and 10. However, it does not disclose the multiplier is an exclusive-OR gate. The McGuffin reference teaches the multiplier is an exclusive-OR gate (see Col. 2, lines 48-57 and Figure 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Hatcher-Ishihara wherein the multiplier is an exclusive-OR gate, as taught by McGuffin, in order to provide frequency multiplication.

4. Claims 5-6 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0160740 A1 to Hatcher et al. in view of Ishihara (U.S. Patent Application Publication 2001/0016017 A1) and further in view of McGrath (U.S. Patent Application Publication 2003/0080809 A1).

As to claims 5 and 14, Hatcher-Ishihara discloses the radio frequency down/up conversion circuit as set forth in Claims 4 and 13. However, it does not disclose a chopping switch capable of receiving said differential output signal of said differential RF mixer. The McGrath reference teaches a chopping switch capable of receiving said differential output signal of said differential RF mixer (see page 2, col. 1, paragraph [0014], and Figure 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Hatcher-Ishihara to further comprise a chopping switch capable of receiving said differential output signal of said differential RF mixer, as taught by McGrath, in order to offset drift reduction in amplifiers.

As to claims 6 and 15, Hatcher-Ishihara-McGrath discloses the radio frequency down/up conversion circuit as set forth in Claims 5 and 14 wherein said chopping switch is synchronized to said frequency divider such that said switching switches its internal connections at said LO/N frequency of said frequency divider and in tandem with said frequency divider (Ishihara: see page 3, col. 2, paragraphs [0041] and [0042], and Figure 6; McGrath: see page 2, col. 1, paragraphs [0014] and [0015], and Figure 1).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Bautista et al. (U.S. Patent 6,125,272) discloses method and apparatus providing improved intermodulation distortion protection.

b. Laws (U.S. Patent 5,303,417) discloses mixer for direct conversion receiver.

c. Goff et al. (U.S. Patent 4,931,745) discloses low noise chopper stabilized amplifier and method of operation.

d. Riley (U.S. Patent 4,691,170) discloses frequency multiplier circuit.

e. Schlager et al. (U.S. Patent 5,486,788) discloses chopper stabilized operational transconductance amplifier.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy K Le whose telephone number is 703-305-5660. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on 703-305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Duy Le
July 16, 2004

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